Inside Engineering

SI-GaAs: Entering the Realm of Silicon - *Page 2*

Semi-Insulating Gallium Arsenide substrates are the foundation of the GaAs Integrated Circuit industry. Improvements in High Pressure Liquid Encapsulated Czochralski crystal growth technology have brought the state-of-the-art of SI-GaAs into the realm of Silicon.

Experimental Effort

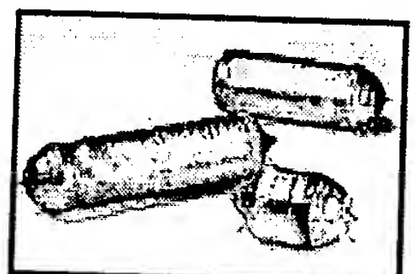

Figure 3

The experimental effort built upon results of the theoretical models. The melt size was incrementally increased from 8 kilograms to 24 kilograms. In addition to hardware modifications suggested by the model, the effects of chamber pressure, seed and crucible rotation rates, and position of the melt within the hot zone were considered. This program resulted in the development of the growth processes listed in Table 1. In each process, the onset of polycrystalline growth has been completely eliminated. A typical crystal from a 17 kg charge is presented in Figure 3.

Table 1: Progression of Charge Sizes

Charge Weight	Single Crystal Weight
15 kg	12.5 kg
17 kg	15.0 kg
21 kg	18.5 kg
24 kg	22.0 kg

The final process yielding a 22 kg crystal from a 24 kg melt results in approximately 400, 100mm substrates per boule. This represents almost a five fold increase in yield per growth run as compared to our baseline 8 kg process.

The success of the crystal growth program at M/A-COM gives us confidence that further advances in boule size can be realized in the future. The charge weights of SI-GaAs which are currently being successfully pulled are comparable to small scale silicon production. Our results indicate that over the next several years, charge sizes comparable to the Silicon industry will be the norm.

Electrical Properties

The electrical properties of SI-GaAs are governed by a balance between background shallow donor and acceptor impurities with the native deep donor defect EL2. As such the resistivity of the substrate is given by:

$$\rho^{-1} \sim \frac{N_{EL2}}{\sum N_a - \sum N_d} \quad \text{where:} \quad \sum N_a > N_{EL2} - \sum N_d$$

for semi-insulating behavior to be observed. In this representation, N_{EL2} is the concentration of the deep donor EL2, $SumN_a$ is the sum of all shallow acceptors, and $SumN_d$ is the sum of all shallow donors.

In the early days of SI-GaAs, the mechanisms which controlled the electrical properties of the material were not understood. It was found that stoichiometry played a critical role in determining the concentration of EL2 [3]. With this realization, most producers of SI-GaAs focused efforts on gaining control of the GaAs synthesis process to obtain the desired stoichiometry in a reproducible manner. For the most part, the role of impurities in determining the electrical properties of the material produced was ignored. From the above relationships, it is clear that background impurity concentrations play as key a role as stoichiometry in determining the substrates properties.

Impurities are primarily introduced by two paths:

- Impurities contained in the raw materials used in the growth process, and
- Impurities introduced during the growth process.

Since the electrical properties are determined by the balance ($SumN_a$-$SumN_d$), it is not only the particular impurities in a given raw material which is of concern but, also the interactions these impurities will have with the impurities contained in other raw materials used in the process. A focus on impurity interactions has resulted in a significant improvement in control over the electrical properties of the material produced as exhibited in Table 2 and Figure 4.

Table 2: Evolution of the Electrical Properties of SI-GaAs

	1988	**1995**
Average Resistivity (ohm-cm)	1.03×10^8	3.02×10^7
Standard Deviation	2.71×10^8	2.60×10^7
Average Mobility (cm^2/V-s)	6243	7371
Standard Deviation	1624	347

Data from M/A-COM's Materials Database

The data of Table 2 indicates an order of magnitude reduction in the standard deviation of the resistivity of the material grown. Likewise, the standard deviation in the electron mobility has been improved by a factor of ~5. The graphic depiction of this data in Figure 4 illustrates the pronounced improvements in the electrical properties of material being produced today. The increase in the electron mobility indicates that SI-GaAs substrates are considerably purer than they were a decade ago.

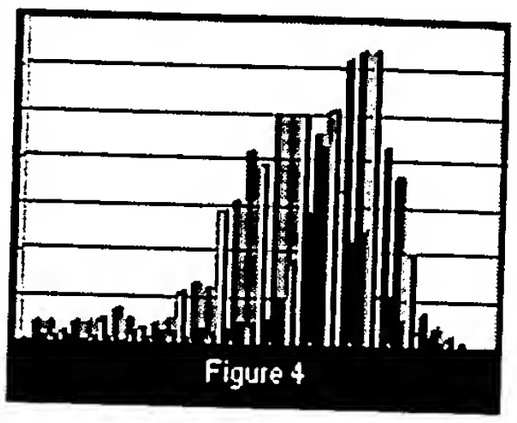
Figure 4

Conclusions

The dramatic improvements in the electrical properties of SI-GaAs substrates coupled with the maturity of GaAs-IC processing has virtually eliminated the substrate from affecting device characteristics. The boule to boule and within boule uniformity has dramatically improved since the early years of GaAs. These attributes are only now allowing IC FABs to question the efficacy of their qualification procedures.

The improved electrical uniformity of material has changed the motivation of increasing melt and boule sizes. The motivation was to decrease boule qualification costs; now it is to obtain cost-effective manufacturing of the material itself. The GaAs industry is truly moving toward the manufacturing realm of the Silicon industry. Materials effects no longer contribute significantly to device performance, allowing diminished qualification costs and the ability to purchase wafers as a commodity.

Acknowledgment

The author is grateful for the support the Defense Production Act, Title III Program "SI-GaAs Wafers" for the support which has allowed these achievements to be realized.

References and Notes

1. See for Example: J.P. Tower, R. Tobin, P.J. Pearah, and R.M. Ware, "Interface shape and crystallinity in LEC GaAs," J. Crystal Growth 114 (1991) 665.
2. CAPE Simulations, Inc. 888 Worcester St. Wellesley MA 02181 USA (617) 237-3225.
3. See for example: J. Lagowski and H. C. Gatos, "Nonstoichiometric Defects in GaAs and the EL2 Bandwagon," Thirteenth International Conference on Defects in Semiconductors, ed. L.C. Kimerling and J.M. Parsey, The Metallurgical Society of AIME, Warrendale, PA, 1985.

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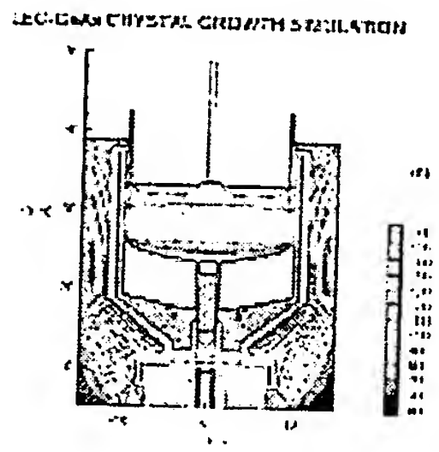
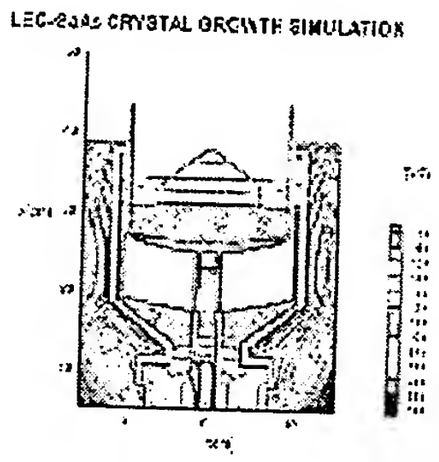
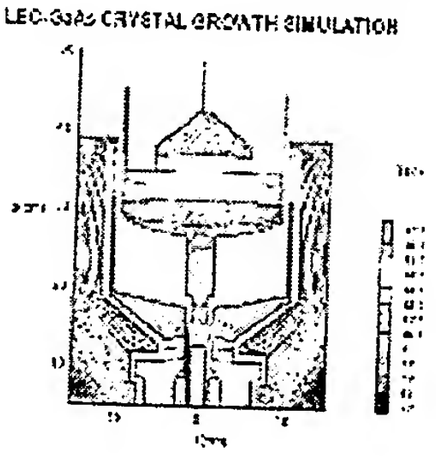


Semi-Insulating Gallium Arsenide substrates are the foundation of the GaAs Integrated Circuit industry. Improvements in High Pressure Liquid Encapsulated Czochralski crystal growth technology has brought the state-of-the-art of SI-GaAs into the realm of Silicon.

Gallium Arsenide integrated circuit technology was born with the development of undoped semi-insulating Gallium Arsenide (SI-GaAs) in 1979. This material was produced by the High Pressure Liquid Encapsulated Czochralski growth technique resulting in 2 and 3 inch diameter crystals yielding 30 wafers per boule. There was little understanding of what parameters were critical to control in the production of this material. The bulk resistivity varied over several orders of magnitude and electron mobility was low indicating a lack of control over both impurity incorporation and the stoichiometry of the material. This in turn lead to deleterious effects in device fabrication. In epitaxial growth, impurity outdiffusion would adversely affect control over layer characteristics, while in ion implantation based processes, implant activation and uniformity would vary from ingot to ingot. The variation observed in the starting material was further amplified by the immature device processing technologies being used at the time.



To reduce the effect of variability caused by the substrate material most users developed an ingot qualification procedure. In general, these procedures would consist of subjecting wafers from the seed and tail end of each ingot to extensive testing. Often implant activation and implant uniformity were the key gating criteria which would be used for boule evaluation. It was tacitly assumed that all wafers between the seed and tail would display similar results as those tested. The need for qualifying material lead to the development of two prevalent thoughts in the use of SI-GaAs: (1) IC FABs purchase boules not wafers, and (2) large boules are required to diminish substrate qualification cost.



Significant progress has been made in the ensuing years in terms of the control over critical materials parameters. These improvements have lead to a level of reproducibility and the trend towards the abandonment of these costly qualification procedures. Increased ingot size is now motivated by cost effective production, as in the silicon industry, rather than a means of reducing qualification costs. The following will detail some of the improvements made in substrate materials over the past years.

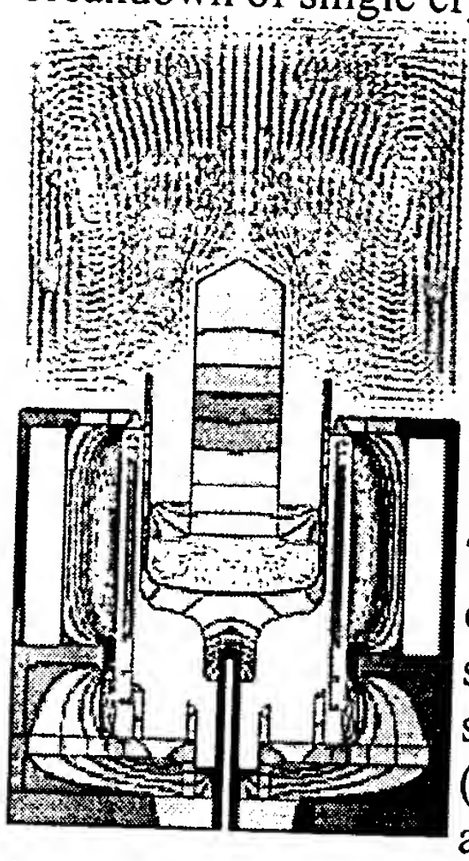
Crystal Growth Development

Crystal growth of SI-GaAs over the past seventeen years has experienced significant progress. The two and three inch production has given way to 100 and 150mm crystal growth. Today, over 65% of the

North American usage of GaAs is 100mm diameter. Though the diameter of material grown has been increasing, the yield of single crystal substrates per growth run has seen minimal progress. Historically the length of single crystal material has been roughly proportional to the diameter of the crystal being grown. The onset of polycrystalline growth has limited the amount of usable material per boule. At M/A-COM, we have undertaken a development effort to maximize the yield of 100mm crystals from large melts. The aim of this large melt development effort is to produce entirely single 100mm diameter crystals from melt sizes in excess of 20 kilograms. To achieve this goal, a program which tightly couples a theoretical exploration of the growth environment with an extensive experimental effort has been undertaken.

Finite Element Modeling

Our hypothesis to increase the yield of single crystal grown from a given melt size was that the breakdown of single crystal growth was linked to the morphology of the crystal/melt interface. It has been demonstrated that a concave morphology at the periphery of the crystal leads to polycrystalline growth [1]. To control the morphology of this interface, a clear understanding of the heat transfer mechanisms in the growth system is required. This process knowledge would allow for modification of the growth environment with predictable results. To gain an understanding of the heat transfer in the growth systems, quasi steady state finite element simulations of the growth process were developed. The development of these theoretical models of our crystal growth systems was conducted by CAPE, Inc. [2].



The finite element models considered the detail geometry and thermal properties of our crystal growth systems. To accurately calculate the heat transfer in the system, conductive, convective and radiative heat transfer was considered. Three stages of the crystal growth process were modelled: growth of the shoulder (early in growth), growth of the initial section of the body (full diameter growth) and growth at the end of the body section. It is during this later stage of growth that polycrystalline growth is often encountered.

Results of these calculations are presented in Figure 1. Figure 1(a) displays growth of the shoulder section. At this stage of growth the interface morphology is convex, a stable growth configuration. As growth proceeds, Figure 1(b), the interface is found to develop a sigmoidal nature. An unfavorable interface morphology then develops, Figure 1(c). as the sigmoidal interface shape develops a concavity at the periphery of the growing crystal. The models successfully predicts the point at which we statistically see the onset of polycrystalline growth.

Progression of Charge Sizes	
Charge Weight	Single Crystal Weight
15 kg	12.5 kg
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Building upon this base, changes to the growth environments were explored. The effect of these changes on the crystal/melt interface were quantified with the aim of identifying an optimized growth environment. This effort culminated in the simulation displayed in Figure 2. This model of a , 24 kilogram melt, considers an optimized environment for growth from large melts.

Experimental Effort

The experimental effort built upon results of the theoretical models. The melts size was incrementally increased from 8 kilograms to 24 kilograms. In addition to hardware modifications suggested by the

model, the effects of chamber pressure, seed and crucible rotation rates, and position of the melt within the hot zone were considered. This program resulted in development of the growth processes listed in Table 1. In each process, the onset of polycrystalline growth has been completely eliminated. A typical crystal from a 17 kg charge is presented in Figure 3.

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Electrical Properties

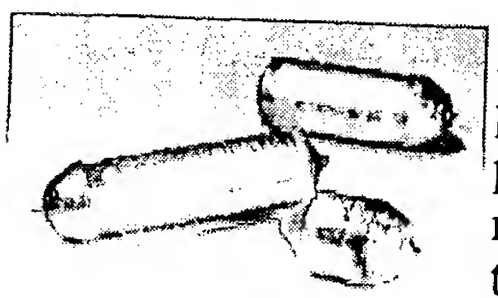
The electrical properties of SI-GaAs are governed by a balance between background shallow donor and acceptor impurities with the native deep donor defect EL2. As such the resistivity of the substrate is given by:

$$\rho^{-1} \sim \frac{N_{EL2}}{\sum N_a - \sum N_d}$$

where:

$$\sum N_a > N_{EL2} - \sum N_d$$

for semi-insulating behavior to be observed. In this representation, NEL2 is the concentration of the deep donor EL2, SNa is the sum of all shallow acceptors, and SNd is the sum of all shallow donors.



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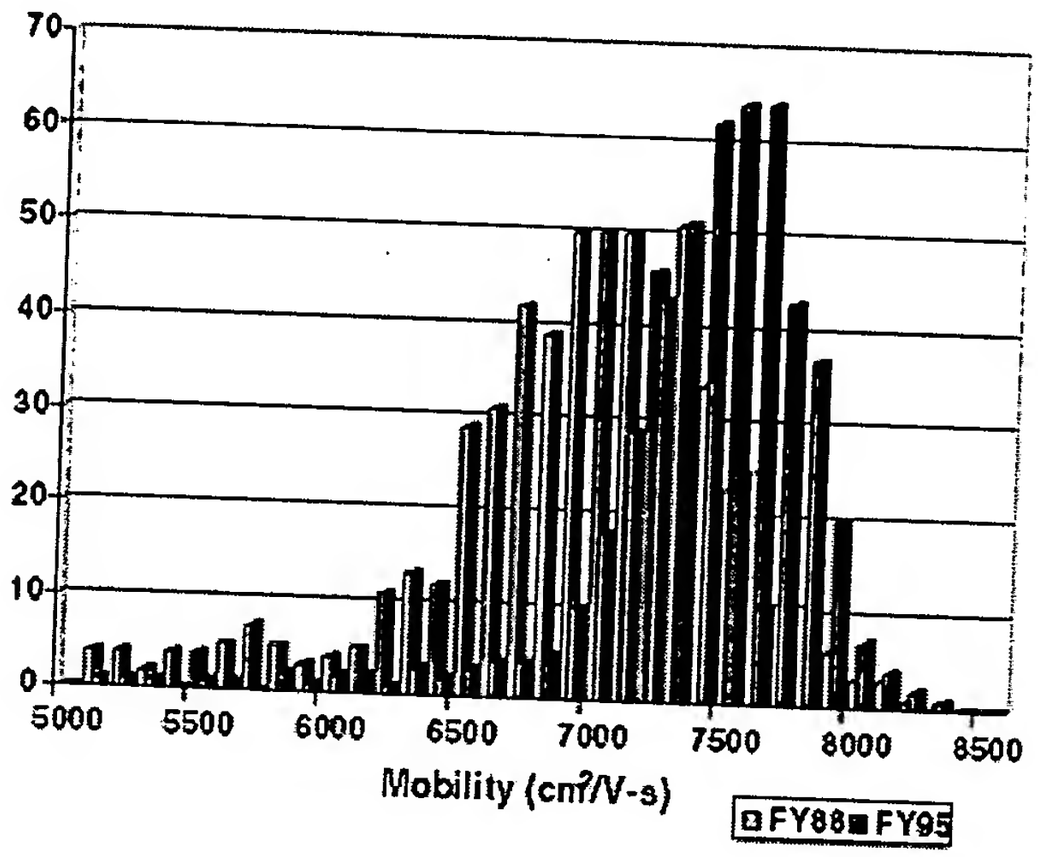
Since the electrical properties are determined by the balance (SNa-SNd), it is not only the particular impurities in a given raw material which is of concern but, also the interactions these impurities will have with the impurities contained in other raw materials used in the process. A focus on impurity interactions has resulted in a significant improvement in control over the electrical properties of the material produced as exhibited in Table 2 and Figure 4.

Evolution of the Electrical Properties of SI-GaAs		
	1980	1995
Average Resistivity (W-cm)	3.02x107	1.03x108
Standard Deviation	2.71x108	2.60x107
Average Mobility (cm2/V-s)	7371 ⊠	6243



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Inside Engineering

Growth and Properties of Very Large Crystals of Semi-insulating Gallium Arsenide - *Page 3*

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- Control Of Crystal Diameter

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- Electrical Properties
- Conclusion & Future Program
- Acknowledgements
- References

Stress

During growth by LEC steep thermal gradients are established in the gallium arsenide crystal. For example vertical temperature gradients measured during growth were found to be 60-80°C/cm.[6]. The resulting stresses cause dislocations and slip and leave frozen-in strain in the crystal.

Relief of this strain can cause crystals to crack. This is avoided by annealing the crystals before grinding or cutting operations are carried out.

The stress due to radial gradients was shown to be at a maximum at a vertical position about two thirds of the encapsulant depth from the melt surface [4]. These stresses are caused by the heat flux from the crystal into the oxide. Since this flow is reduced the stress in the crystals is also diminished.

Electrical Properties

The electrical properties of semi-insulating gallium arsenide are determined by a balance between a defect level EL2, which is a deep donor, and chemical impurities, principally sulfur and carbon.

The concentration of EL2 is determined by the melt stoichiometry and that of the chemical impurities by the purity of the raw materials, handling practices and the growth environment.

High purity semi-insulating gallium arsenide typically has electrical resistivity in the range $1\text{-}5*10^7$ ohm.cm, and electron mobilitiy >7000 $cm^2/v.sec$.

Results of Hall measurements on three crystals over 500mm long are given in Table I.

TABLE I
Electrical Properties of Large GaAs Crystals

Crystal	Resistivity(10^7 ohm.cm)		Mobility(cm^2/v.sec)	
	seed	tail	seed	tail
1	2.3	2.6	7888	7865
2	3.5	2.7	7899	7561
3	2.0	5.1	7777	7568

When higher resistivities are required this can be achieved by controlled carbon doping and this process was described by W.M.Higgins et al. [7].

Conclusion & Future Program

Modification of the thermal environment of the MR 15/25 high pressure puller has enabled us to grow very large (22kg) crystals of high quality semi-insulating gallium arsenide. The equipment, with minor modification, could be employed for growing 4 inch diameter crystals up to 42kg, 90cm long. However 22kg is close to the limit which can be handled manually. Growth of significantly larger crystals will require robotic handling systems.

The process is being applied to the CI 358 pullers, where it will enable an increase in charge size from eight to fourteen kilograms. This represents an increase from 100 to 200 wafers per boule.

Acknowledgments

The authors acknowledge the support of the Title III pro-gram Office under contract # F33733-94-C-1019.

The support and forbearance of Dr. D. Carlson is also gratefully acknowledged.

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